Single Channel ESD Protection Device in 0402 Package

Check for Samples: TPD1E10B09

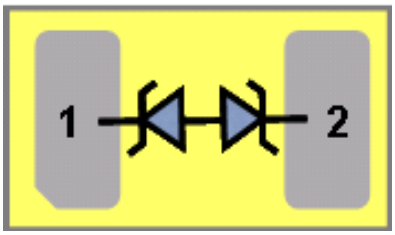
FEATURES

- **Provides System Level ESD Protection for Low-voltage IO Interface**
- **IEC 61000-4-2 Level 4**
  - **±20kV (Air-Gap Discharge),**
  - **±20kV (Contact Discharge)**
- **IEC 61000-4-5 (Surge): 4.5A (8/20µs)**
- **IO Capacitance 10pF (Typ)**
- **R_{DYN} 0.5Ω (Typ)**
- **DC Breakdown Voltage ±9.5V (Min)**
- **Ultra Low Leakage Current 100nA (Typ)**
- **13V Clamping Voltage (Max at I_{PP} = 1A)**
- **Industrial Temperature Range: –40°C to 125°C**
- **Space Saving 0402 Footprint (1mm x 0.6mm x 0.5mm)**

APPLICATIONS

- **Cell Phones**
- **eBook**
- **Portable Media Players**
- **Digital Camera**
- **Set-top-box**
- **Printers**
- **Handheld Electronics**

DEVICE CONFIGURATION



DESCRIPTION

The TPD1E10B09 is a single channel ESD protection device in a small 0402 package. The device offers ±20KV IEC air-gap, ±20KV contact ESD protection, and has an ESD clamp circuit with a back-to-back diode for bipolar or bidirectional signal support. The 10pF line capacitance is suitable for a wide range of applications supporting data rates up to 500Mbps. Typical application areas for the TPD1E10B09 are audio lines (microphone, earphone and speakerphone), SD interface, keypad or other buttons, and VBUS pins of USB ports (ID).

The 0402 package is industry standard and convenient for component placement in space saving applications. The TPD1E10B09 is characterized for operation over ambient air temperature of -40°C to 125°C.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	10000	Tape and reel	TPD1E10B09DPYR	A_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
	Operating temperature range	-40	125	°C
	Storage temperature	–65	155	°C
	IEC 61000-4-2 contact ESD		±20	kV
	IEC 61000-4-2 air-gap ESD		±20	kV
I_{PP}	Peak pulse current (tp = 8/20 µs)		4.5	A
P_{PP}	Peak pulse power (tp = 8/20 µs)		90	W

ELECTRICAL CHARACTERISTICS

T_A = –40ºC to 85ºC unless otherwise specified

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	Pin 1 to 2 or Pin 2 to 1			9	V
I_{LEAK}	Leakage current	Pin 1 = 5 V, Pin 2 = 0 V			100	nA
VClamp1,2	Clamp voltage with ESD strike on pin 1, pin 2 grounded.	I_{PP} = 1 A, tp = 8/20 µSec(1)			13	V
		I_{PP} = 5 A, tp = 8/20 µSec(1)			17	
VClamp2,1	Clamp voltage with ESD strike on pin 2, pin 1 grounded.	I_{PP} = 1 A, tp = 8/20 µSec(1)			13	V
		I_{PP} = 5 A, tp = 8/20 µSec(1)			20	
R_{DYN}	Dynamic resistance	Pin 1 to Pin 2(2)		0.5		Ω
		Pin 2 to Pin 1(2)		0.5		
C_{IO}	IO capacitance	V_{IO} = 2.5 V		10		pF
$V_{BR1,2}$	Break-down voltage, pin 1 to pin 2	I_{IO} = 1 mA	9.5			V
$V_{BR2,1}$	Break-down voltage, pin 2 to pin 1	I_{IO} = 1 mA	9.5			V

(1) Non-repetitive current pulse 8/20 us exponentially decaying waveform according to IEC61000-4-5
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I_{PP} = 10A and I_{PP} = 20A.

TYPICAL CHARACTERISTICS

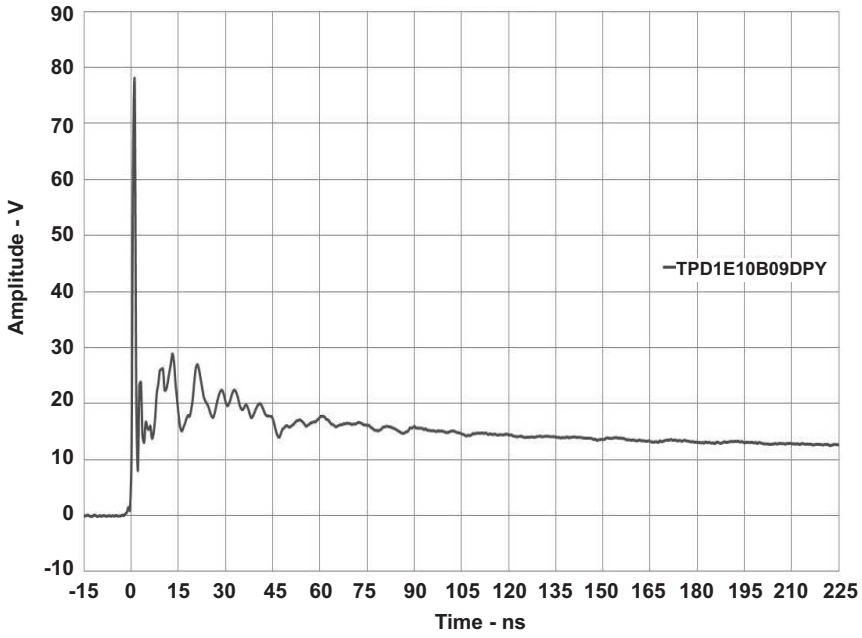


Figure 1. ESD Clamp Voltage +8KV Contact ESD

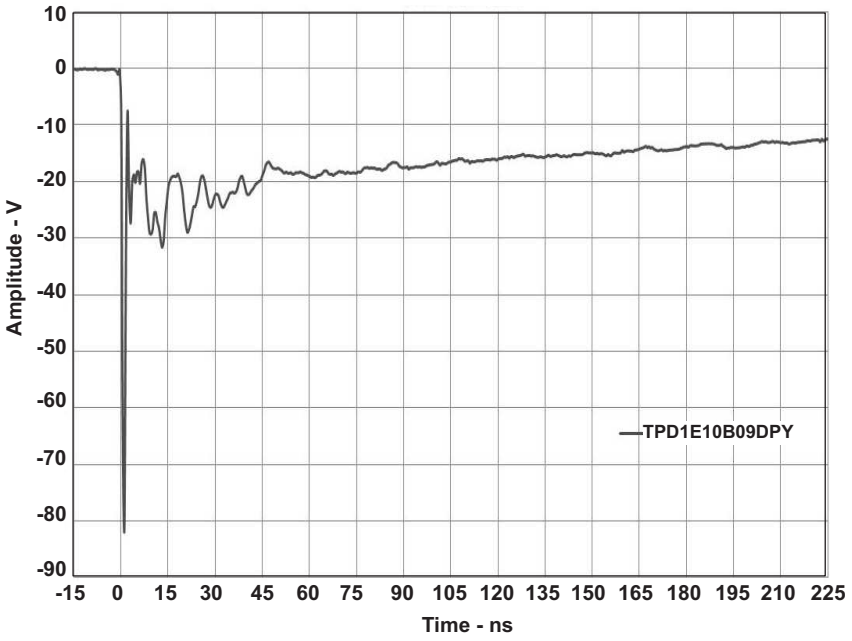


Figure 2. ESD Clamp Voltage –8KV Contact ESD

TYPICAL CHARACTERISTICS (continued)

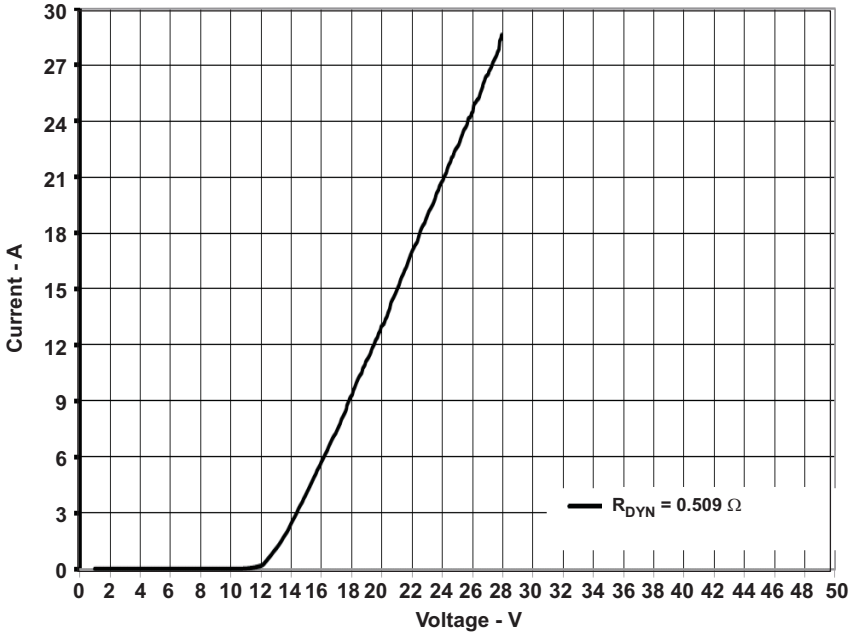


Figure 3. Transmission Line Pulse (TLP) Waveform Pin1 to Pin2

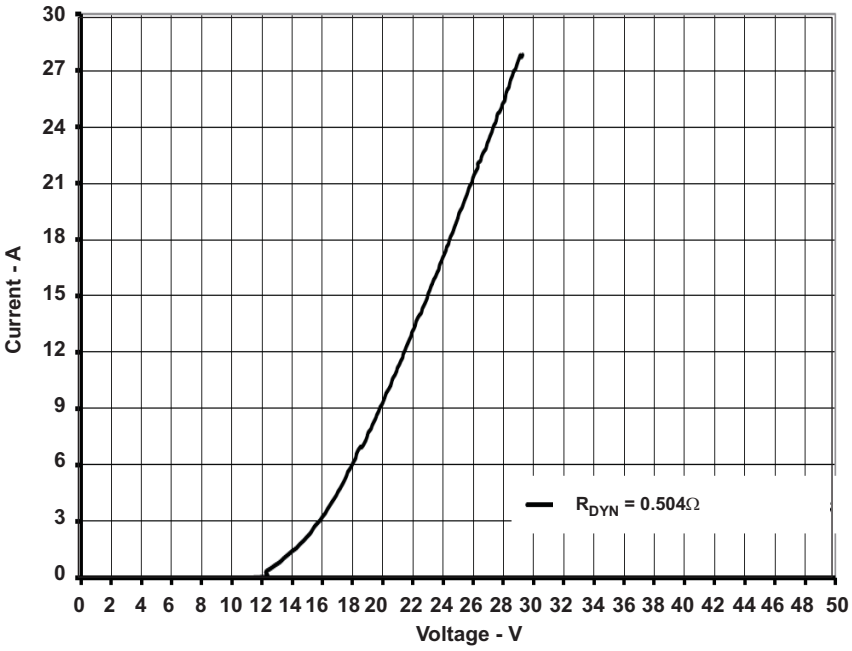


Figure 4. Transmission Line Pulse (TLP) Waveform Pin2 to Pin1

TYPICAL CHARACTERISTICS (continued)

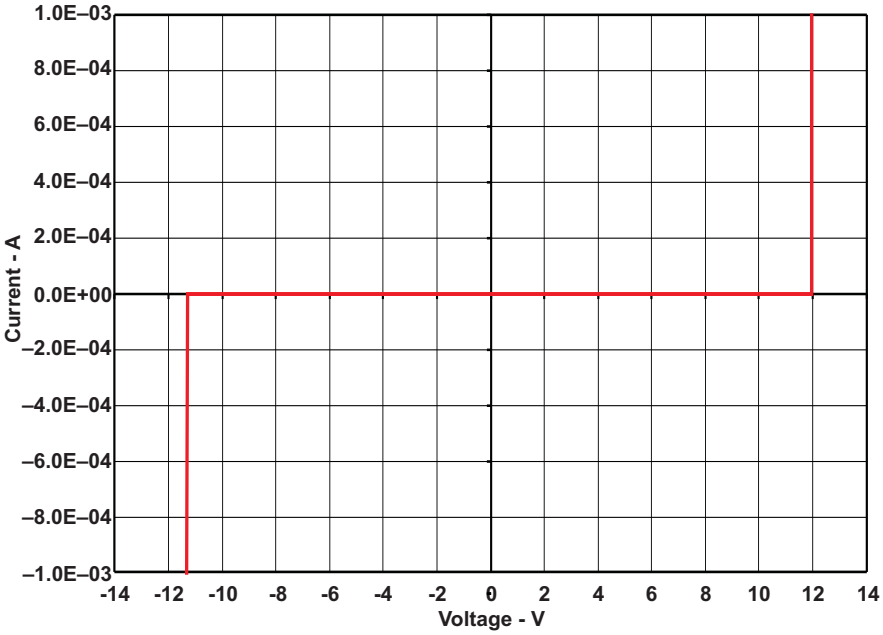


Figure 5. IV Curve

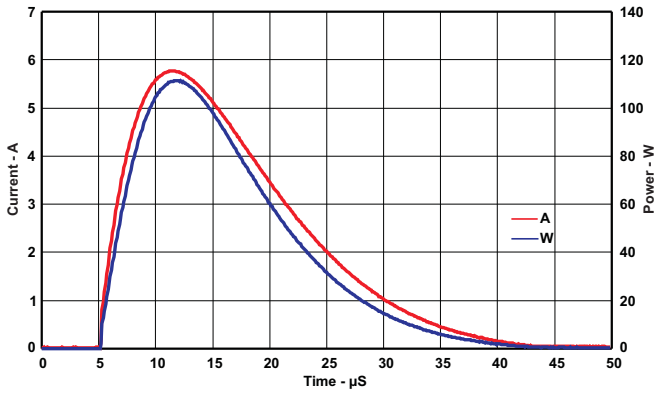


Figure 6. Positive Surge Waveform 8/20µs

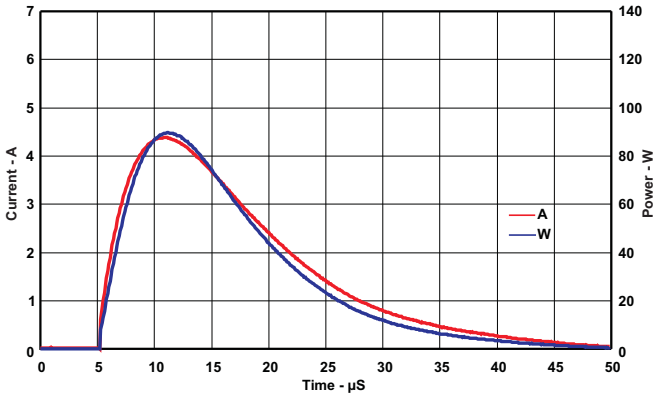


Figure 7. Negative Surge Waveform 8/20µs

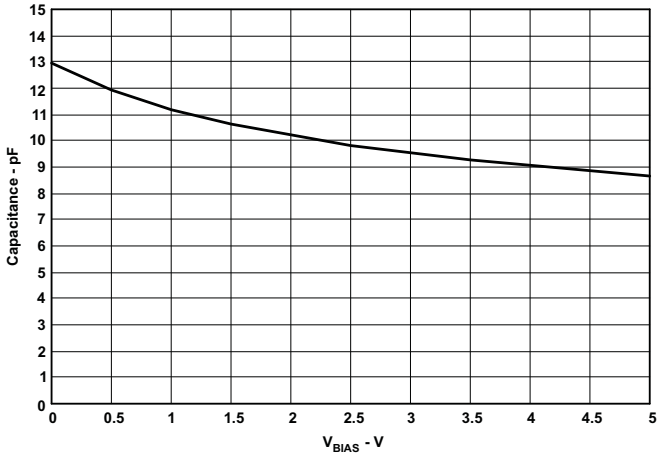


Figure 8. Pin Capacitance Across V_{BIAS}

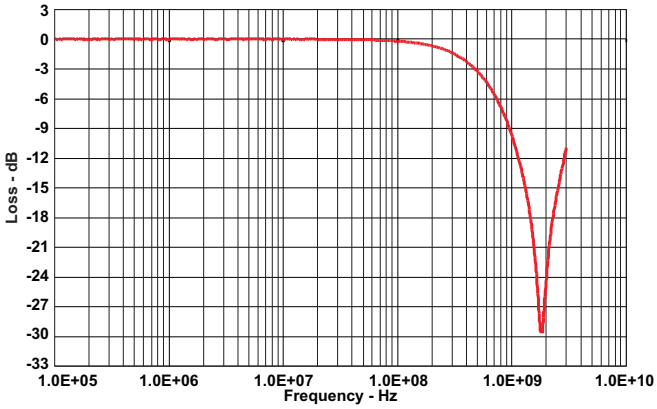


Figure 9. Insertion Loss

APPLICATION INFORMATION

The TPD1E10B09 is a single channel back-to-back diode that protects a single bi-directional signal line from Electro static discharge and surge pulses. Since its bi-directional, it protects signals that have positive or negative polarity. During normal operation, the diode behaves as a 10 pF capacitance to ground. Board layout is critical for optimal performance of any diode.

Placement: The diode should be placed very close to the external connector for optimal performance. Ideally, the diode should be placed on the line that it is protecting.

Layout: The diode pin 1 should be right over the signal line that it protects. There should a thick and short trace from pin 2 to ground. An example is shown below.

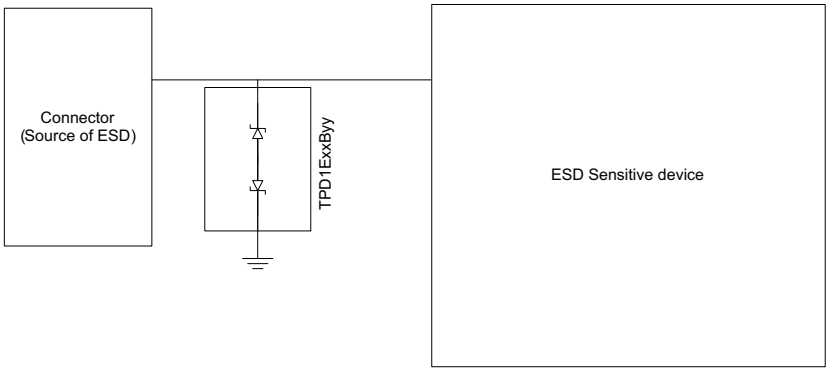


Figure 10. Application Schematic

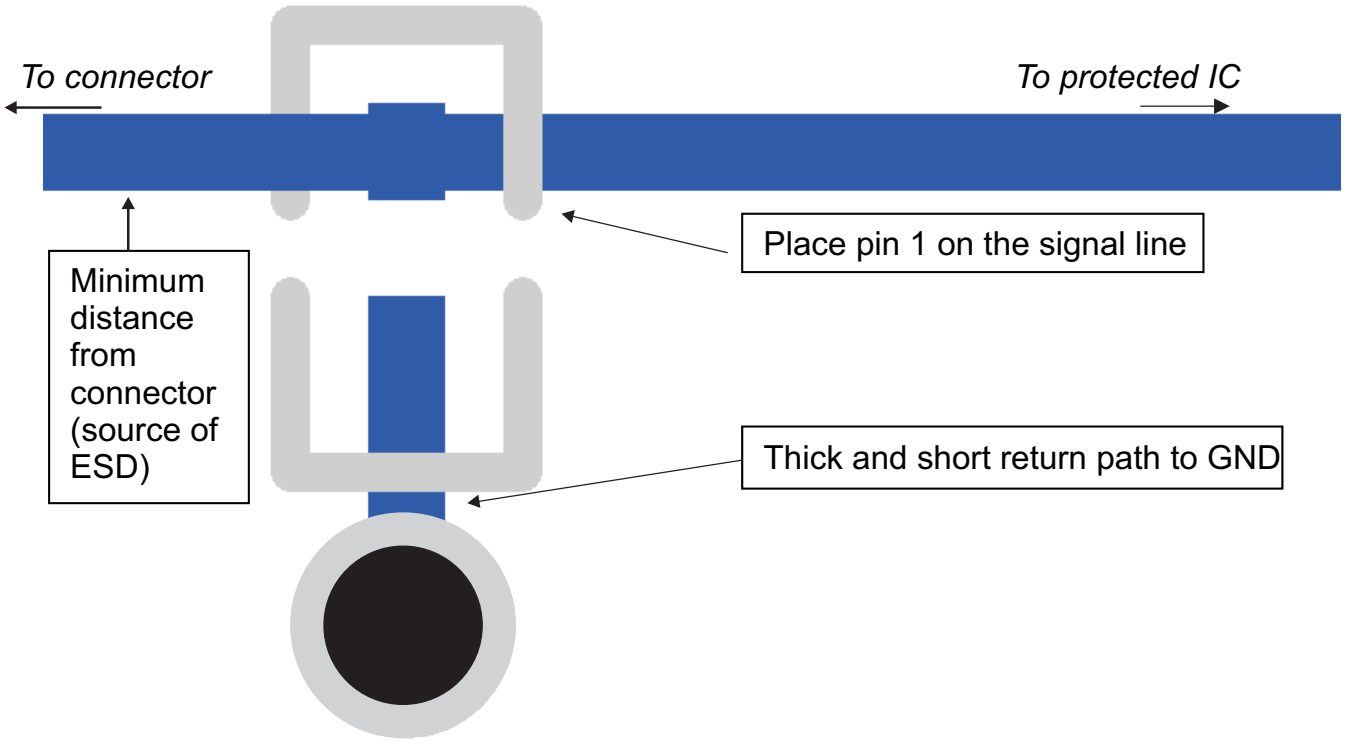


Figure 11. Layout Example

REVISION HISTORY

Changes from Original (February 2012) to Revision A **Page**

- Updated FEATURES. 1
- Added graphs to TYPICAL CHARACTERISTICS section. 5
- Added APPLICATION INFORMATION section. 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPD1E10B09DPYR	ACTIVE	X2SON	DPY	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

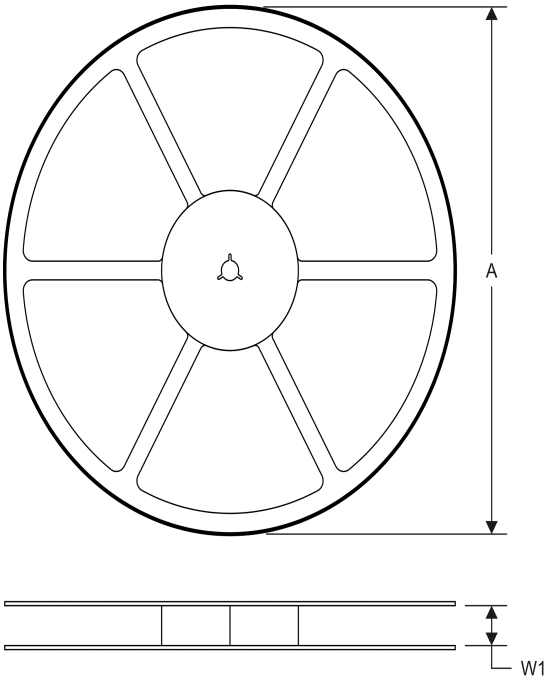
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

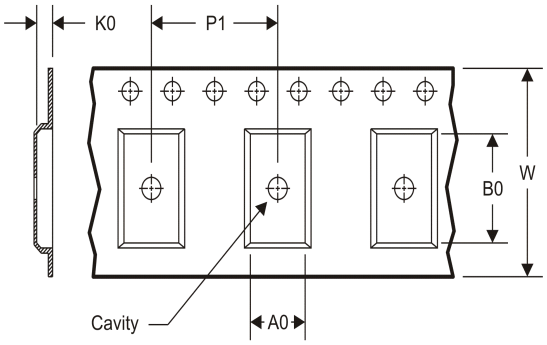
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



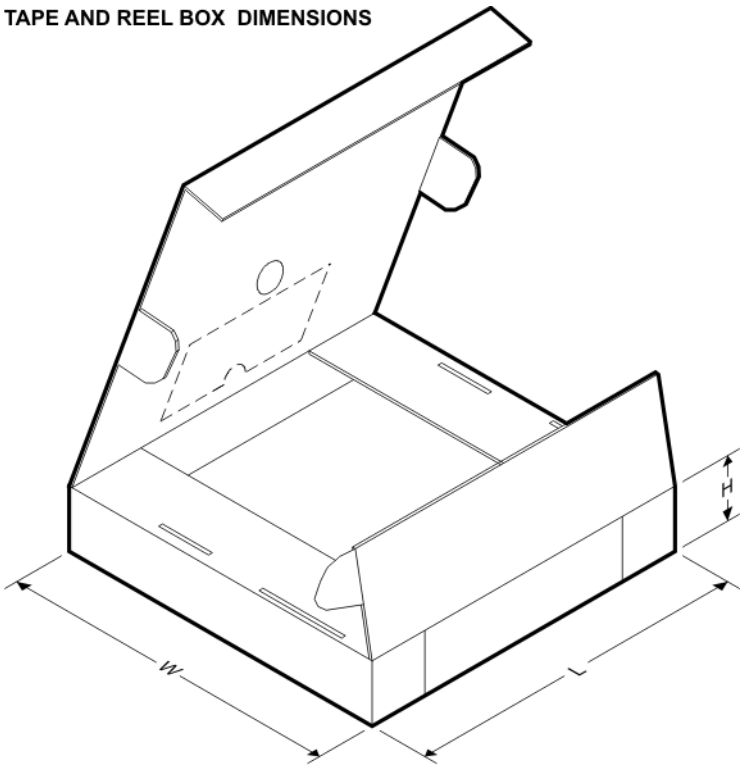
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E10B09DPYR	X2SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	4.0	8.0	Q1

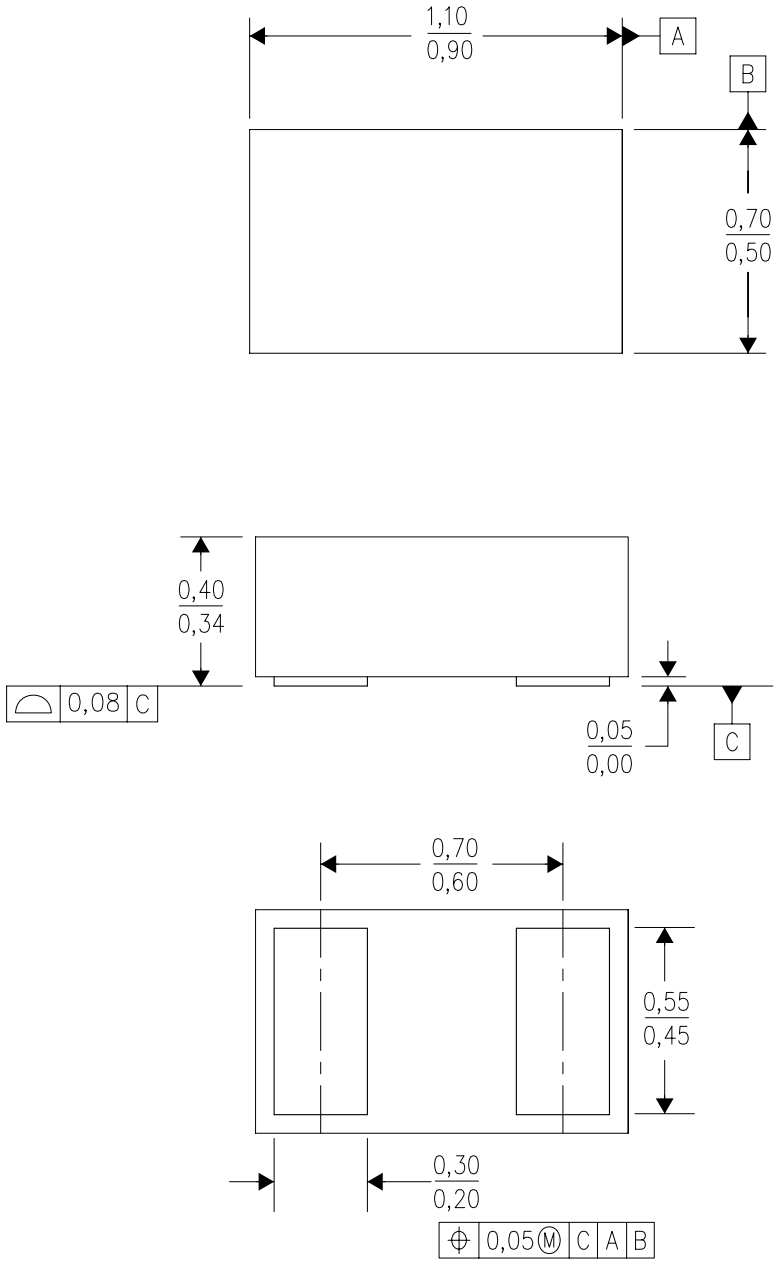
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E10B09DPYR	X2SON	DPY	2	10000	180.0	180.0	30.0

DPY (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

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